

AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently amended) A method for sharing a plurality of interrupt inputs associated with a processor among a plurality of interrupt sources, which generate interrupt requests, comprising the steps of:

mapping each of the interrupt requests from the plurality of interrupt sources to each of the plurality of interrupt inputs of an interrupt controller that receives the interrupt requests ~~and prioritizes the servicing of received requests;~~

assigning priorities to each of the plurality of interrupt inputs by the interrupt controller; and

selectively enabling interrupt requests from each of the plurality of interrupt sources to be received at one or more of the plurality of interrupt inputs based on the assigned priorities of the interrupt inputs.

2. (Previously presented) The method of claim 1, wherein the step of selectively enabling comprises:

determining a value of control bits respectively associated with each mapped interrupt request / interrupt input combination; and

selectively enabling mapped interrupt request/ interrupt input combinations according to the respective control bit values.

3. (Previously presented) The method of claim 1, wherein the step of selectively enabling comprises:

a) determining a value of a control bit associated with a mapped interrupt request / interrupt input combination;

b) selectively enabling mapped interrupt request / interrupt input combination according to the associated control bit value; and

c) repeating steps a and b until control bit values for all mapped interrupt request / interrupt input combinations are determined and enabled/disabled accordingly.

4. (Original) The method of claim 2, further comprising setting the control bit values according to user preferences.

5. (Original) The method of claim 4, further comprising dynamically modifying the control bit values according to user preferences.

6. (Original) The method of claim 2, further comprising defining the control bit values according to system requirements, said system comprising the processor, at least one interrupt source, and at least one interrupt input.

7. (Currently amended) A system for sharing a plurality of interrupt inputs associated with a processor among a plurality of interrupt sources, which generate interrupt requests, comprising:

logic that maps each of the interrupt requests from the plurality of interrupt sources to each of the plurality of interrupt inputs of an interrupt controller that receives the interrupt requests ~~and prioritizes the servicing of received requests;~~

logic that assigns priorities to each of the plurality of interrupt inputs by the interrupt controller; and

logic, which is operatively connected to the logic that maps, that selectively enables interrupt requests from each of the plurality of interrupt sources to be received at one or more of the plurality of interrupt inputs based on the assigned priorities of the interrupt inputs.

8. (Previously presented) The system of claim 7, wherein the logic that selectively enables comprises:

logic that determines a value of control bits respectively associated with each mapped interrupt request / interrupt input combination; and

logic, which is operatively connected to the logic that determines, that selectively enables mapped interrupt request / interrupt input combinations according to the respective control bit values.

9. (Previously presented) The system of claim 7, wherein the logic that selectively enables comprises:

logic that determines a value of a control bit associated with a mapped interrupt request / interrupt input combination;

logic, which is operatively connected to the logic that determines, that selectively enables interrupt requests between the mapped interrupt request / interrupt input combination according to the associated control bit value; and

logic, which is operatively connected to the logic that selectively enables, that advances the logic that determines and the logic that selectively enables until control bit values for all mapped interrupt request / interrupt input combinations are determined and enabled/disabled accordingly.

10. (Previously presented) The system of claim 8, further comprising logic, which is operatively connected to the logic that determines, that sets the control bit values according to user preferences.

11. (Previously presented) The system of claim 10, further comprising logic, which is operatively connected to the logic that sets, that dynamically modifies the control bit values according to user preferences.

12. (Previously presented) The system of claim 8, further comprising logic, which is operatively connected to the logic that determines, that defines the control bit values according to system requirements, said system comprising the processor, at least one interrupt source, and at least one interrupt input.

13. (Previously presented) The system of claim 8, wherein the logic that selectively enables comprises, for each mapped interrupt request /interrupt input combination, a logical AND for ANDing each interrupt source with a respective control bit value.

14. (Currently amended) A system for sharing a plurality of interrupt inputs associated with a processor among a plurality of interrupt sources, which generate interrupt requests, comprising[[:]], for each of said plurality of interrupt inputs:

a plurality of logical ANDs, each corresponding to an interrupt source, the corresponding interrupt source providing an interrupt request signal to the corresponding logical AND to interrupt the processor;

a plurality of control bits each corresponding to an interrupt source and each respectively providing a control bit value to the corresponding logical AND, wherein, based on the control bit value, a corresponding interrupt request signal is provided at an output of the corresponding logical AND; and

a logical OR arranged to indicate, to the interrupt inputs of an interrupt controller that receives the interrupt requests and ~~prioritizes the servicing of received requests~~ assigns priorities to each of the plurality of interrupt inputs, the presence of a corresponding interrupt

request signal from at least one output of the plurality of logical ANDs, wherein the plurality of logical ANDs are operatively connected to the logical OR.

15. (Original) The system of claim 14, further comprising a register for storing the control bit values.

16. (Original) The system of claim 14, further comprising logic that sets the control bit values according to user preferences.

17. (Original) The system of claim 16, further comprising logic that dynamically modifies the control bit values according to user preferences.

18. (Original) The system of claim 14, further comprising logic that defines the control bit values according to system requirements, said system comprising the processor, at least one interrupt source, and at least one interrupt input.

19. (Original) The system of claim 14, wherein the processor is part of a microcontroller unit.

20. (Original) The system of claim 14, wherein the number of interrupt sources is greater than the number of interrupt inputs.

21. (Currently amended) A method for sharing a plurality of interrupt inputs associated with a processor among a plurality of interrupt sources, which generate interrupt requests, comprising the steps of:

mapping each of the interrupt requests from the plurality of interrupt sources to each of the plurality of interrupt inputs of an interrupt controller that receives the interrupt requests ~~and prioritizes the servicing of received requests;~~

assigning priorities to each of the plurality of interrupt inputs by the interrupt controller; and

selectively enabling and disabling interrupt requests from each of the plurality of interrupt sources to be received at one or more of the plurality of interrupt inputs,

wherein an interrupt request corresponding to at least one of the plurality of interrupt sources is enabled for one of the plurality of interrupt inputs and said interrupt request corresponding to the said one of the plurality of interrupt sources is disabled for another one of the plurality of interrupt inputs.

22. (Previously presented) The method of claim 21, wherein the step of selectively enabling comprises:

a) determining a value of a control bit associated with a mapped interrupt request /interrupt input combination;

b) selectively enabling and disabling interrupt requests between the mapped interrupt request /interrupt input combination according to the associated control bit value; and

c) repeating steps a and b until control bit values for all mapped interrupt request /interrupt input combinations are determined and enabled/disabled accordingly.

23. (Currently amended) A system for sharing a plurality of interrupt inputs associated with a processor among a plurality of interrupt sources, comprising:

logic that maps each of the interrupt requests from the plurality of interrupt sources to each of the plurality of interrupt inputs of an interrupt controller that receives the interrupt requests ~~and prioritizes the servicing of received requests;~~

logic that assigns priorities to each of the plurality of interrupt inputs by the interrupt controller; and

logic, which is operatively connected to the logic that maps, that selectively enables and disables interrupt requests from each of the plurality of interrupt sources to be received at one or more of the plurality of interrupt inputs,

wherein an interrupt request corresponding to at least one of the plurality of interrupt sources is enabled for one of the plurality of interrupt inputs and said interrupt request corresponding to said one of the plurality of interrupt sources is disabled for another one of the plurality of interrupt inputs.